Low Noise Front-End Amplifier Dedicated to Monitor Very Low Amplitude Signal from Implantable Sensors

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Abstract
This paper describes a low-noise, low-power and low-voltage analog front-end amplifier integrated in implantable electronic devices and dedicated to very low amplitude signal acquisition. Low noise and low DC offset are obtained by means of Chopper Stabilization (CHS) technique. In addition, due to adding a rail to rail input stage, low power supply (1.8V) and wide common mode input range (0-1.8V) are achieved also. It features a gain of 51dB and a bandwidth of 4.5 kHz. The equivalent input noise is about 56nV/√Hz.

I. Introduction
A large number of applications require an ultra low-amplitude signal measurement module, such as implantable sensors in biomedical applications intended to monitor several neuromuscular activities. Among these devices, bladder controller that allows to measure volume of the urine and adjust stimulation parameters when necessary, is an important rehabilitation application, as shown in figure 1 [1]. Its analog front-end interface, Volume-Monitoring Device (VMD) is used to sense the nerve signal that contains the volume information of the bladder.

![Bladder control](image)

Figure 1. Block diagram of the global system dedicated to bladder control

Nerve signal $V_n$, of which the amplitude is very low and generally ranged from 1 to 10 μV, will be submerged in noise of the conventional CMOS two stages topology Opamp. Hence, it needs to be first weakly amplified by a Low Noise Amplifier (LNA) to overcome 1/f noise and to rise the needed signal above the noise level of the following instrumentation amplifier (IA) which amplifies the signal with a programmable gain and rejects the common mode signal.

For electronic implantable system applications, the dominant noise source is often the 1/f noise component of the differential input stage. The use of increased processing steps and reduced gate dimensions associated with scaling generally leads to increase the 1/f noise level. CHopper Stabilization (CHS) technique is well-known for reducing the 1/f noise and DC offset. The low-noise amplifier circuit implementation based on chopper technique had been reported in [2]. However the circuits discussed in previous papers all worked under at least 4V supply voltage and the signal bandwidth was limited in few hundred Hz. As in the implantable system applications, the main energy is transmitted from outside the body through the skin, thus the supply voltage and power consumption of system should be minimised. In addition, the bandwidth of nerve signal can be up to 10 kHz, the signal bandwidth of the analog front-end in the VMD should be improved also. In this paper, we present a complete analog front-end system which works well under single 1.8V supply voltage and realizes a wide common mode input range by using a rail-to-rail low noise amplifier. And since the implantable system should be fully integrated, the modulating clock signal is generated on-chip by a voltage controlled oscillator.

The organization of the paper is as follows: Section II describes the proposed low-voltage low-noise CHS amplifier circuit. The measurement results of the prototype chip and conclusion are given in sections III and IV respectively.

II. Circuit Implementation

1. Block diagram
The block scheme of the system is shown in figure 2. The selective amplifier is composed of two stages, a rail-to-rail low-noise preamplifier and a bandpass filter. There are two advantages of this structure: first, a wide common mode input range can be achieved by the rail to rail amplifier, without impairing the linearity of Gm-C filter. Second, the input transconductance value in BPF does not need to be very high to realize a high DC gain, thus it is not necessary to compensate the offset which comes from high transconductance value of input pairs.
2. Rail-to-rail Modulator

The input modulator can be realized by simple passive modulators which is composed of four cross-coupled analog switches that are controlled by two non-overlap clocks having frequency. In order to guarantee an adequately low switch resistance in a low voltage environment, a bootstrapped switch that inspired from [3] can be used. The switch is conceptually a single NMOS transistor, as shown in figure 3.

During the off phase, $\phi$ is high. The switch $S_3$ discharges the gate of $M_1$ to ground. Meanwhile, $V_{DD}$ is applied across capacitor $C$ by the switches $S_1$ and $S_2$. And the switches $S_4$ and $S_5$ isolate the transistor $M_1$ from $C$ while it is charging. In the $\phi$ phase, the switches $S_1$, $S_2$ and $S_4$ are off while the switches $S_3$, $S_5$ are on. The capacitor $C$ whose voltage has been charged to $V_{DD}$ on the previous phase behaviors as a battery across the source-gate of the transistor $M_1$ during this phase. It turns on transistor $M_1$ and enables gate of $M_1$ to track the input voltage shifted by $V_{DD}$, keeping the gate-source voltage unchanged regardless of the input signal. The clock double circuit that consists of two transistors $M_2$ and $M_3$ and capacitors $C_1$ and $C_2$ are added to operate the switches $S_1$ to $S_5$.

2. Low Noise Preamplifier

The preamplifier consists of a rail-to-rail OTA followed by a transimpedance stage. As the power supply is only 1.8V, in order to improve signal dynamic range and common mode input range, a rail-to-rail input stage is used. The DC gain of the amplifier equals to $G_{m1}/G_{m2}$, where $G_{m1}$ and $G_{m2}$ are the transconductance value of the rail to rail OTA and the transimpedance stage respectively. The bandwidth of the amplifier should be high enough to ensure that little gain and phase distortion will be introduced to the system.

A. Rail to Rail OTA

The rail-to-rail input stage is realized by placing two N- and P-type differential pairs in parallel. Constant $g_m$ is obtained by means of two maximum current select (MCS) circuits, which are made of transistors from MP09 to MP20 in figure 4. The MCS circuit compares two input currents, eg. $i_{p1}$ and $i_{p2}$, that come from N-pair and P-pair input stage (not given out in figure 4) respectively, and output the larger one. This is feasible because the two different input currents will lead to either current source (MP09 , MP10) or current sink (MN11, MN12) lost their saturation region, and not act as a constant current source again. Thus as long as the input pairs are tuned with an equal $g_m$, the $g_m$ value of the OTA will be universal constant. Another advantage of the MCS circuit is that it outputs a stable DC operation current no matter which region the input pairs locate on. This makes the common mode feedback (CMFB) circuit that is necessary for the full differential system working well.

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modulator. Its block scheme is present in figure 5(a). Due to lack of virtual grounds and low impedance nodes, the gm-C filter are sensitive to parasitic capacitors. Therefore, we should add a automatic tuning circuit in the BP filter to lock its center frequency \( f_c \) with \( f_{\text{chop}} \). The automatic tuning methods in continuous time filter have been discussed in many papers. But for the CHS amplifier, the deviation of \( f_{\text{chop}} \) itself will not introduce significant impacts on the performance of CHS. The critical point of tuning in CHS is to make \( f_c \) tracking with \( f_{\text{chop}} \), rather than fix it with a reference clock. Thus we can use an on-chip oscillator which uses the same resonator structure with the BPF as shown in figure 5 b). The tuning error will only come from mismatching rather than the parasitic parameters. This structure reduces the complexity of the whole system. It is especially important in this application whose modulator clock should be generated on-chip. The GNL (Non-linear Conductance) is used to guarantee oscillation and regulate amplitude[4].

![Figure 5](image)

**III. Simulation & Experimental Results**

The experimental chips have been fabricated in CMOS 0.35 \( \mu \)m technology. The layout is shown in figure 6. Its core area size is around 0.52 mm\(^2\). The measured gain of the rail-to-rail input amplifier is shown in figure 7. The variation of gain is smaller than 5%, better than the conventional rail-to-rail amplifiers. The DC gain of the low noise preamplifier equals to 26dB and the –3dB frequency is about 1.2 MHz, much larger than \( f_{\text{chop}} \) (40 KHz in our case). The measured oscillator Chopper frequency (\( f_{\text{chop}} \)) and center frequency (\( f_c \)) are around 37 KHz. Quality factor \( Q \) is specified at 4, thus the signal bandwidth can be up to 4.5 KHz. The simulated input referred equivalent noise is 56\( \text{mV}/\sqrt{\text{Hz}} \). The static power consumption of the total acquisition front-end is only 775\( \mu \)W.

![Figure 6](image)

**IV. CONCLUSION**

A fully integrated low-voltage analog front-end dedicated to implantable monitoring applications is presented. The chopper modulation technique was chosen to reduce the low frequency noise and DC offset in CMOS opamp. The low supply voltage and wide common mode input range are realized by using a rail to rail low noise preamplifier. This amplifier was originally designed for biomedical applications, however it can be used for any low frequency applications to monitor ultra low amplitude signal.

![Figure 7](image)

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**REFERENCE**


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