A fast passive data transmission system for an implantable telemeter

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Abstract
As part of a close-loop neuroprosthesis for preventing incontinence, naturally-occurring nerve signals will be used to control the stimulation. Two neural signals are to be relayed from the implant. Power is provided to the implant by radio-frequency induction. We are developing data transmission by impedance modulation at a higher bit rate than used previously. This has the advantage of simplicity within the implant and small power loss. This system can already transmit at 160 kbits/s with a 4 MHz carrier and coil-coil separations up to more than one diameter (70mm). The major design problems are described.

1. Introduction
In 1986, Hoffer & Sinkjaer [1] proposed that the neural signals picked up by cuff electrodes could be used as inputs for neuroprostheses. To make this feasible, we developed an ENG Telemeter [2] which amplifies the ENG from one tripolar cuff and transmits the analogue signal from the body on a frequency-modulated 380 kHz carrier. This device has demonstrated the clinical possibilities of naturally-occurring signals [3]. We are now developing an implanted device for closed-loop control that combines a selective nerve stimulator and two ENG telemetry channels. This paper is about the telemetry sub-system.

To simplify the implant, we propose to use impedance modulation (i.e. a passive not active method). We have used this before for transmitting pulses of length 8 µs on a 3.8 MHz carrier [4,5]. Tang et al. [6] use a variation that they call load-shift keying for pulse code modulation to send EMG data at 36 kbits/s on a carrier of 8.75 MHz (ratio carrier frequency / bit rate = 243). Their group has since increased the bit rate to 200 kbit/s (ratio 44).

We investigated whether, if the modulation was synchronised with a carrier at 4 MHz, two ENG signals, each sampled at 10 ksamples/s, could be transmitted for a wide range of coil-coil coupling.

2. Modulation

Figure 1 shows the external transmitter circuit (L1C1) coupled to the implant circuit (L2C2) from which power is drawn to the load, which represents the implant electronics. Bits are sent by closing, or not closing, the Switch at regular bit intervals (6 µs here). Figure 2 shows the pulses applied to operate the switch, the effect on the voltage across C3, and the transient increase in transmitter current, seen as the voltage across C1.

2. Design Considerations
Figure 3 shows a block diagram of the sub-system.
The system is made of eight functional blocks. At the implant side, the analogue signals are converted into 10-bit binary data by the A/D converter, encoded, and converted into a serial pulse train. The flow is synchronised by clock A from the Clock A Recovery circuitry, which is synchronous with the carrier. At the transmitter side, outside the body, the modulated current is extracted via a capacitor divider. After amplitude demodulation and Clock B Recovery, the bit train is restored, the digital words are decoded, and converted back to the analogue signals.

2.1 How short can the switch pulse be?

Simulation and experiment show a sufficient pulse width is ½ an RF period. However, to make maximal change in the primary current by the short pulse, the time where the modulation starts is crucial: it is best if the switch FET conducts when the voltage across C2 passes zero (Figure 4).

2.2 Clock A recovery

To define the start position of the pulse, a synchronising clock must be recovered from the incoming RF itself, but this is interrupted by the modulation. To solve the problem, a long pulse blanks the cycles that may have small amplitude or abnormal phase (compared to the transmitter drive) and then the blanking pulses are ORed with the unblanked RF to produce a hybrid clock (Figure 5).

2.3 Demodulation

Two factors cause difficulty: (1) The coupling of the two coils decreases quickly with increasing spacing which leads to large variation of modulation index (Figure 6).
To achieve fast bit rate, the pulse interval is less than the transient period. To detect bits at large spacing, the design of the demodulator is critical.

### 2.4 Clock B Recovery

The pulse train at the output of the demodulation block is irregular but Clock B is needed to sample this data stream. A digital phase-locked loop reproduces the clock from the data stream. Because the RF transmitter and the PLL are both derived from the same oscillator, errors caused by mismatches of the frequency, that would occur with an analogue PLL, are reduced.

### 2.5 Encoding and decoding

To maximise the transmission rate, the data should be encoded with the fewest possible additional bits that allow word synchronisation, and the data flow should not be interrupted. Our method uses only two extra bits per pair of data samples (i.e. 20+2 bits). Each extra bit is the parity bit for 10 data bits.

The decoder has 22 counters (Figure 7), representing all the possible ways that the stream could be divided into words. For each bit of the stream, the probability that both bits in the positions of the parity bits will be right by chance is \( \frac{1}{4} \) unless the data is synchronous, when the parity will be correct (assuming no transmission errors). A positive result of the parity test causes the counter to count up 1, a negative result causes it to count down by 4. Each counter can not count below 00000\(_2\) or above 10100\(_2\). This means that after a few words, the probability that more than one counter has a large count is very small, so the counter with the largest count shows the correct synchronisation and this operates the latch that passes the word to the D/A converters.

### 3. Summary

This method has the advantages that most of the complexity is external; that the loss of power is small; and a high data rate is possible. We expect that it will work at 222 kbits/s (carrier frequency/bit rate = 18), which is a sample rate of 10.1 kHz on two channels, and that at minimal coupling, coil-coil spacing will be 70 mm ($k \approx 0.015$).

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#### References


