Amplifier Structure for Neural Signal Recording

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Abstract

An ASIC for recording ENG signals has been developed. The basic blocks for a microelectronic solution including an auto-polarised high pass filter and amplifier with band pass filter can be combined on two different structures for implementing a full system amplifier. The design of and results from more important blocks and full system are presented. The circuit has been designed considering to work with cuff electrodes, and performances such as low power consumption, low noise and low offset, without the use of external components, are important characteristics. A 4 channel implantable recording system can be built just repeating some of the structures here presented.

1. Introduction

It has been suggested that natural sensors have some appropriate properties for control purpose on restoring the mobility in paralysed members [1,2]. Many different systems has been developed for recording ENG signals to obtain information across natural sensors. Nevertheless, the characteristics of neural signals (very small signal to noise ratio, bandwidth at small frequencies and electrode offset) make the system's implementation too complex and it is very difficult to find an implantable version. The most important characteristics of the signal conditioning circuitry are the bandwidth, small noise and high gain.

In this paper the basic blocks needed for a microelectronic solution are presented. Two important blocks such as high pass filter to attenuate the signal contamination due to EMG basically and low noise differential input amplifiers to implement the required gain are developed. In an implantable system implementation an additional gain should be added in order to send out digital data for signal post processing. Other important consideration are related with power consumption and area that must be kept as small as possible.

For the design of these blocks the following specifications have been considered: input signals in the range from 5μV to 5mV, bandwidth from 100Hz to 5KHz, and an offset of 100mV due to electrodes must be removed. Next, the basic blocks implementation will be presented and after due to the wide input range two system implementations will be built and experimental results will be reported.

2. High Pass Filter

A High Pass Filter (HPF) with a cut-off frequency in 100Hz is needed with a zero at the origin to eliminate the DC component. The simpler HPF is the RC with a transfer function \( \frac{RCS}{RCS + 1} \), the pole defines the cut-off frequency that in this case is fixed to 100Hz. For implementing without external components an internal 20pF capacitor (feasible in a CMOS technology) and 80MΩ resistor are needed. This high resistor is not possible to implement with a 2KΩ/\( \Omega \) poly due to large area needed (\( \sim 1 \text{ sqmm} \)) and tolerance. Then, a MOS P transistor auto-polarised in the sub-threshold region will be used. The polarisation circuit makes the filter independent with temperature, power supply and also from technological parameters.

![Fig. 1: Schema of the implantable stimulator](image_url)
continuous voltage is removed with a maximum offset of 5V limited by the technology.

3. Amplifier with Band Pass filter (ABPF)

The second basic block, through which the loop gain will be fixed, is a differential amplifier with a band pass between 100Hz and 5KHz. The block is designed around a DDA [3] characterised for having two differential inputs. One is used for the signal capture and the second one to implement a negative and positive feedback paths. The negative feedback is used to define the gain with an attenuating resistor in a similar way as in a typical OTA configuration. In this way the high cut-off frequency will be defined.

The positive feedback path is used to implement a high pass filter with an ideal inverter integrator. This makes that final stage has a zero at the origin that eliminates the offset from input and DDA. With the loop gain and the integrator's time constant the low cut-off frequency is defined to be in 100Hz. The integrator is implemented with a simple operational amplifier and, for the RC defining the time constant, the structure used is the HPF with a 25pF capacitor and the same polarisation circuit for the PMOS transistor.

In this way it is possible to obtain an amplifier with low noise and low residual offset because the integrator on the positive feedback path removes the direct DDA offset and internal flicker noise.

4. Structure for full amplifier

Two different structures are required due to the wide input range and to the thermal noise introduced by the RC filter greater than the lower input signal. Therefore, the full input range (5µV to 5mV) will be divided into two sub-ranges one going from 5µV to 0.5mV and the second from 50µV to 5mV.

The structures presented are based on different combination of the above basic blocks described for implementing filtering action and gain. For the treatment of signals in the sub range between 50µV to 5mV a minimum loop gain of 60 dB is required to digital transformation of the analog signal for a later post processing. Three stages have been used for this implementation as shown in Fig. 2 each one of them having a specific task to fulfil.

1. HPF, the main purpose of this block is to attenuate frequency components outside the signal bandwidth then, gain is not introduced but electrode offset is eliminated. The cut-off frequency will be fixed to 100Hz.

2. The ABPF will be implemented to have 34dB gain within the bandwidth with a lower and upper cut-off frequencies of 100Hz and 5.5KHz respectively.

3. A standard OpAmp to add 26 dB to the direct loop gain adapting the output voltage to the input range of the ADC.

Fig. 2: Structure for a conditioning circuitry for the high input range

This scale is characterised for a fourth order band pass filter with 60dB of gain in the direct loop.

The second structure proposed is implemented to be used with input signals in the sub-range from 5 to 500µV, in this case a total loop gain of 80 dB is desirable. The filter at the input is substituted by an ABPF because the thermal noise generated by the PMOS transistor used as resistor is bigger than the input signal, then an ABPF with 34dB of gain is used as first stage. The second stage is another ABPF, used to eliminate the residual offset introduced for the OTA in the feedback path from the first stage the gain for this stage is 23dB. Also a third OpAmp with 23dB of gain will be necessary to accommodate the output level to the input for the ADC. In this structure the offset from electrode is limited to 100mV according with initial specifications. Moreover the 80dB of gain a fifth order filter is implemented with a slope up of 40dB/dec and 60dB/dec in the slope down at 100Hz and 5.5KHz respectively.

5. Results and Conclusions

The basic blocks and amplifier structures previously described have been implemented with a CMOS 0.7µm technology a microphotograph of the designed circuit is shown in Fig. 3. All blocks and basic structures are implemented separately for testing purposes, DDA, HPF with buffer, HPF with ABPF for first scale, ABPF and ABPF for second scale. Different interconnections among
these blocks are possible allowing a full system implementation.

![Microphotograph of the developed ASIC](Fig_3.png)

All the test and characterisation of the different blocks has been carried out with 8 samples. The characterisation of the purposed structure for the low input range needs some additional external amplification because of the limited resolution of available oscilloscope. The equipment used for testing are HP8904A wave generator, Keithley 2700 multimeter and Yokogawa D708E oscilloscope all controlled by PC through GPIB bus. For Bode diagram a frequency sweep from 10Hz to 40KHz was done picking up 28p/dec.

The first block tested was the RC that implements the HPF with 20dB/dec slope up, with cut-off frequency at 130Hz, and removing the dc component.

Results for the amplifier structure in the range from 50μV to 5mV are: 58dB total loop gain, a fourth order band pass filter between 140-5600Hz decaying with 40dB/dec for the two cut-off frequencies and the rejected offset from electrodes is 5V. Finally the CMRR, measured with 1KHz signal, is 94dB and a deviation of ±15Hz for the low cut off frequency is got.

Table 1 summarise the main parameters for the amplifier structure for the low range from 5 to 500μV. Additional external amplification is required to allow an oscilloscope capture.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation</th>
<th>Experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>130-5500Hz</td>
<td>120-5600Hz</td>
</tr>
<tr>
<td>Slope up</td>
<td>40dB/dec</td>
<td>40dB/dec</td>
</tr>
<tr>
<td>Slope down</td>
<td>60dB/dec</td>
<td>60dB/dec</td>
</tr>
<tr>
<td>Gain</td>
<td>80dB</td>
<td>79.9dB</td>
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<tr>
<td>DDA CMRR</td>
<td>90dB</td>
<td>90dB@1KHz</td>
</tr>
<tr>
<td>Noise rms</td>
<td>7.6μV</td>
<td>6.9μV*</td>
</tr>
</tbody>
</table>

* Measure equipment with limited bandwidth to 5KHz

Table 1: Results for recording circuit range from 5 to 500μV.

The power consumption for the full system including the polarised sub-threshold MOS circuit and bias for DDA, is less than 900μW, calculated from simulation.

A transient response to a simulated neural signal of 50 μV using the low range amplifier structure is shown in Fig.4.

![Transient response to a 50 μV input](Fig_4.png)

With these amplifier structures it is possible to build an implantable circuit (four channels i.e.) for neural signal recording just including some of them.

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**References**

