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A LABORATORY FES SYSTEM FOR MODULATED CONTROL OF THE LOWER EXTREMITIES

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ABSTRACT

Functional control of the lower extremities by electrical stimulation utilizing a stored pre-programmed set of control sequences will be used to improve the quality of walking in persons with neuromuscular impairment. A laboratory-based system is described that will permit an operator to select modulated sequences to actuate the limbs in precise coordinated movements with a host/slave processor arrangement and a unique set of output modules which generate the stimulation signals.

INTRODUCTION

Electrical stimulation has been used to activate appropriate muscles of the lower extremities during ambulation to improve the quality of walking in persons with neuromuscular impairment(1-4). Until recently, control has been "on-off", i.e., stimulus parameters are held constant during each period of stimulation. Stanic et al(5) showed that improved performance could be achieved by modulating stimulation to produce a graded response in the stimulated muscles, in their case, the ankle dorsiflexors. Even greater improvement in walking quality can be expected by using modulated control of the larger muscles of the hip and knee.

Selection of modulated control sequences to optimally assist a person with neuromuscular impairment during walking is far from trivial. Models of bipedal gait are not accurate enough to generate the desired control by computer simulation. This means that appropriate control sequences must be determined experimentally in the laboratory for each individual. To arrive at the control sequences in a straight forward, easy to understand, and flexible method in the laboratory setting where time is limited requires a computer system with enough speed and power to handle a number of complicated tasks. The addition of stimulation channels and the capability of handling complicated control algorithms for the eventual likelihood of the closed-loop control of functional electrical stimulation (FES) are also very desirable features not easily attained in traditional stimulation systems. Trnkoczy(6,8) and Strojnik(7) have employed microprocessor based stimulators in their research which allow a pulse train to be modulated in several descrete steps, allowing greater control of limb movement compared to "on-off" type stimulators. Thrope(9) and Buckett(10) have refined even more the use of laboratory computer controlled and microprocessor based stimulators which can modulate functional neuromuscular stimulation. What precipitated the departure from non-computer based stimulation systems for our work was the necessity of changing variables of stimulation for any single pulse or even all pulses during a train of pulses for modulating the stimulation of a motor group being used in the movement control studies described here. A system that has been recently developed to accomplish this is described in this paper.

SYSTEM DESCRIPTION

A block diagram of the system is shown in Figure 1. The heart of the system is a Cromemco System One microcomputer. Control sequences stored in memory can be used to directly control any number of stimulation channels through output modules 1 thru N. Muscle force is modulated by controlling the amplitude and/or duration of each pulse in the stimulation train. Each output module can be connected to a pair of cutaneous or percutaneous electrodes. The stored sequences can also be used to program stimulators implanted inside the body. Multichannel stimulators are now being developed and our system has been designed to be compatible with these stimulators.

Control sequences stored in the microcomputer are easily altered. The stimulation envelope of the channel of control to be changed is displayed on a Modgraph GX100 graphics terminal screen, and the desired change is drawn on the screen by moving the screen cursor with a Houston Instruments Hi Pad digitizing tablet. When the operator is satisfied with the change, the old control sequence is replaced in memory with the new control sequence. An Epson FX80 graphics printer can be used to obtain a hard copy of all of the control sequences at any time.

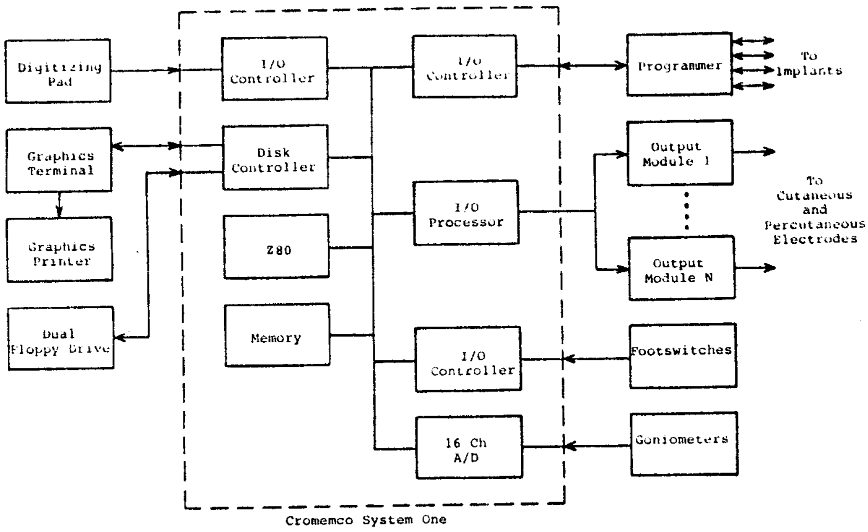

Figure 1. Block Diagram of Rancho Laboratory Stimulation System.

Walking performance is documented by electrogoniometers placed on the knee and ankle and by footswitches that monitor foot/floor contact at the heel, first metatarsal, fifth metatarsal and toe. These data, averaged over one walking trial, can be displayed on the graphics terminal superimposed with the control sequences. A video system and an electromyographic recording system, though not shown in the block diagram, are also available for use on selected walking trials.

Averaged footswitch and goniometric data from any trial can be stored on floppy disks along with the control sequences used on that trial. This will permit us to easily return to a previous control set if subsequent changes lead to a degradation in walking performance.

SYSTEM USER OPERATION

Given a set of control sequences, the patient will be asked to walk with the aid of electrical stimulation along a 10m walkway. The investigative team, consisting of a clinician with extensive experience in bipedal ambulation and an engineer who is knowledgeable in functional electrical stimulation, will determine what changes should be made in the control sequences to improve walking performance. This decision will be made by observing the patient while he/she is walking and correcting these observations with the goniometric, footswitch, and when necessary, electromyographic data. Changes to the control sequences are implemented using the graphics terminal and digitizing tablet as described above. The patient is then asked to walk again with the assistance of the new set of control sequences. This trial and error process is continued as long as necessary (generally over several days of testing) until satisfactory performance has been achieved.

Initial estimates of the control sequences can be obtained in one of two ways. One method is to simply "draw" a priori sequences on the graphics terminal based upon electromyographic records from normals and from ambulatory patients with similar neuromuscular impairments. A second method is to have a physical therapist trained in electrostimulation select appropriate on-off controls for the patient by adjusting the stimulus amplitude, delay from trigger and duration of stimulus train for each stimulation channel. This procedure is done routinely at our hospital with multichannel stimulators used clinically for gait training. When the "best" set of stimulation parameters has been determined by the therapist, they are programmed into the computer and used as a starting point for determination of the modulated sequences.

SYSTEM HARDWARE DESCRIPTION

Host Computer

The Rancho Laboratory Stimulator uses a Cromemco System One computer as the host processor. This S-100 bus system has a Zilog Z80A microprocessor, sixty four thousand bytes of random access memory (RAM), a custom sixteen channel twelve bit analog to digital converter (ADC), two floppy disks, a Modgraph GX100 graphics terminal emulating a Tektronix 4010, a Houston Instruments Hi Pad digitizing tablet and an Epson FX80 graphics printer. The host processor is responsible for: the generation of interactive video graphics for use in the definition of stimulation envelopes and other parameters of stimulation; the generation of data lookup tables corresponding to those stimulation parameters so determined; data acquisition and storage; and communication with a slave processor.

Because of the inherent complexity of the above approach, we decided that it would be more prudent to design a system employing two processors, one to govern overall system performance and a slave processor to handle just waveform generation. To further reduce the overhead to the slave processor and to alleviate the need for supervision during the generation of a biphasic stimulus waveform, intelligent output modules were designed. The use of intelligent output modules is a unique departure from laboratory computer or microprocessor based stimulation systems of the past.

Slave Processor

The slave processor also employs a Z80A microprocessor and is responsible for controlling the specially designed output modules. This arrangement, host and slave, allows each processor to have a full complement of memory and, more importantly, frees the host from the time consuming responsibility of directly controlling the output waveforms for each of the stimulation channels.

The slave processor board chosen was the Input/Output Processor (IOP) from Cromemco. This board consists of a Z80A microprocessor, sixteen thousand bytes of RAM, space for thirty two thousand bytes of programmable read only memory, and an external data, address, and control bus with which it can control devices such as output modules, more memory or other computer peripherals, and it resides as a peripheral on the host processor S-100 bus. The slave processor receives its program and operating instructions as well as the data tables used in the stimulation process over the S-100 bus of the host processor. Since the host computer uses the very popular S-100 bus, it was decided to design the output modules so that each would reside on a single card for the S-100 bus and to adapt the external bus of the IOP to the S-100 bus as well. The output modules which are controlled by the slave processor are very capable pieces of hardware, requiring only basic information about the waveform pulse parameters and a software trigger to start a stimulus pulse. The output module is a memory mapped device and thus looks like an ordinary set of memory locations to the processor. This allows the full complement of memory-referenced instructions of the Z80A microprocessor to be used with the device. The module's base address is switch selectable to reside on any 256 byte page in memory, allowing a large number of these modules to be used in a system with negligible fragmentation of the slave processors memory assignments.

OUTPUT MODULES

In the generation of stimulus waveforms in a microprocessor-based system the most obvious design approach to take is to have the microprocessor directly controlling the output of a stimulus channel by means of an input/output (I/O) port and a digital to analog converter (DAC), and timing the duration of the various levels of DAC output using software timing loops or programmable timers. Although this is a rather straight forward approach, it is very costly to the processor when the number of channels is increased or when the waveforms become more complex. This approach places great demands on the microprocessor's attention since it will likely be responsible for more than just waveform generation. It also requires a great deal of programming skill to prevent variations in computer response to interrupts and to other variables in processing time such that the timing relationships in the output waveform can be guaranteed to be accurate. The output modules in our system were designed to operate in a nearly independent manner to avoid these problems.

The output modules in our system consist of four main sections: five twelve bit wide data latches corresponding to the pre-stimulus current amplitude, positive phase of the biphasic waveform current amplitude, interphase interval amplitude, negative phase amplitude, and the post-stimulus current amplitude; six programmable sixteen bit timers, four of which are used for the duration of positive, interphase, and negative phase intervals and the inter-pulse intervals; timing and control logic; and a twelve bit multiplying DAC and buffer amplifier. The module can thus be set up by the slave processor with the amplitudes corresponding to the five phases of the stimulation waveform by storing twelve bit numbers in the five latches, resulting in one in 2047 amplitude resolution, the length of time for each of the three pulse phases with one microsecond resolution in three of the sixteen bit timers and the length of the inter-pulse interval in the fourth timer. In addition, a vectored interrupt may be generated at the conclusion of any of the above intervals, allowing extremely fast response by the Z80A slave microprocessor to an end-of-pulse or end-of-period event.

Once these values are stored on the module, the microprocessor has only to do a memory write to a location on the board to trigger a stimulus pulse set to occur. All timing, gating, and control functions required to retrieve the twelve bit latch information and regulate the operation of the timers are performed on the module with absolutely no need for processor supervision. Additional pulses can be triggered by simply writing to the start location again. If it is necessary to change parameters such as amplitude or pulse width of the three phases, as will be the case in our application, it can be done easily by waiting for an end-of-pulse interrupt and then modifying the latches and timers. This causes no harm to the interpulse interval timer, thus maintaining stimulus timing integrity.

SYSTEM OPERATION CHARACTERISTICS

The advantages of such a host/slave system with essentially intelligent output modules are that the addition of channels will require only minor modifications to control algorithms and only minor increases in processor time overhead. Each channel addition would entail the insertion of another S-100 bus output module card, setting its address to a unique page in memory and providing it with the proper attention in the operating system. Because the output modules are S-100 bus compatible, it is feasible to use these modules in a number of applications and computer systems.

In our application, the host processor receives information concerning the patterns of stimulation to be applied by each channel via the graphics terminal keyboard and a digitizing tablet and displays the information corresponding to a stimulation sequence in a gait cycle on the graphics screen. Samples of the graphics information presented to the researcher are shown in Figure 2, which depict the envelope definition process for a single channel and a graphics summary of four active channels showing their timing relationships to each other and to left and right heel switch trigger events. Linear and non-linear curve smoothing will modify the data until the researcher is satisfied with the results, after which the host will generate data tables from this information which will then be given to the slave processor over their common S-100 bus communication link.

During stimulation, the host will not be idle but will be using a custom sixteen channel ADC to acquire information from goniometers, and an I/O port to acquire footswitch information for triggering stimulus events. The sixteen channel ADC can acquire a twelve bit number in only six microseconds and can place the result in either a left or right justified sixteen bit word. Left justification is particularly useful during a control situation where accuracy is not as important as fast response. This makes it possible to use only the most significant eight bits of a left justified result as a pointer in a data table lookup algorthm. Right justified results lend themselves directly to math operations requiring twelve bit accuracy. But in either case, no shifts or rotates of the twelve bit result are necessary to get the data in the desired format. The ADC operates by receiving two bytes of information: a channel number and format code in the first byte and a start command in the second byte. The reason for using two bytes was to allow the result format to be changed without initiating another data conversion. The six microseconds are almost transparent to the

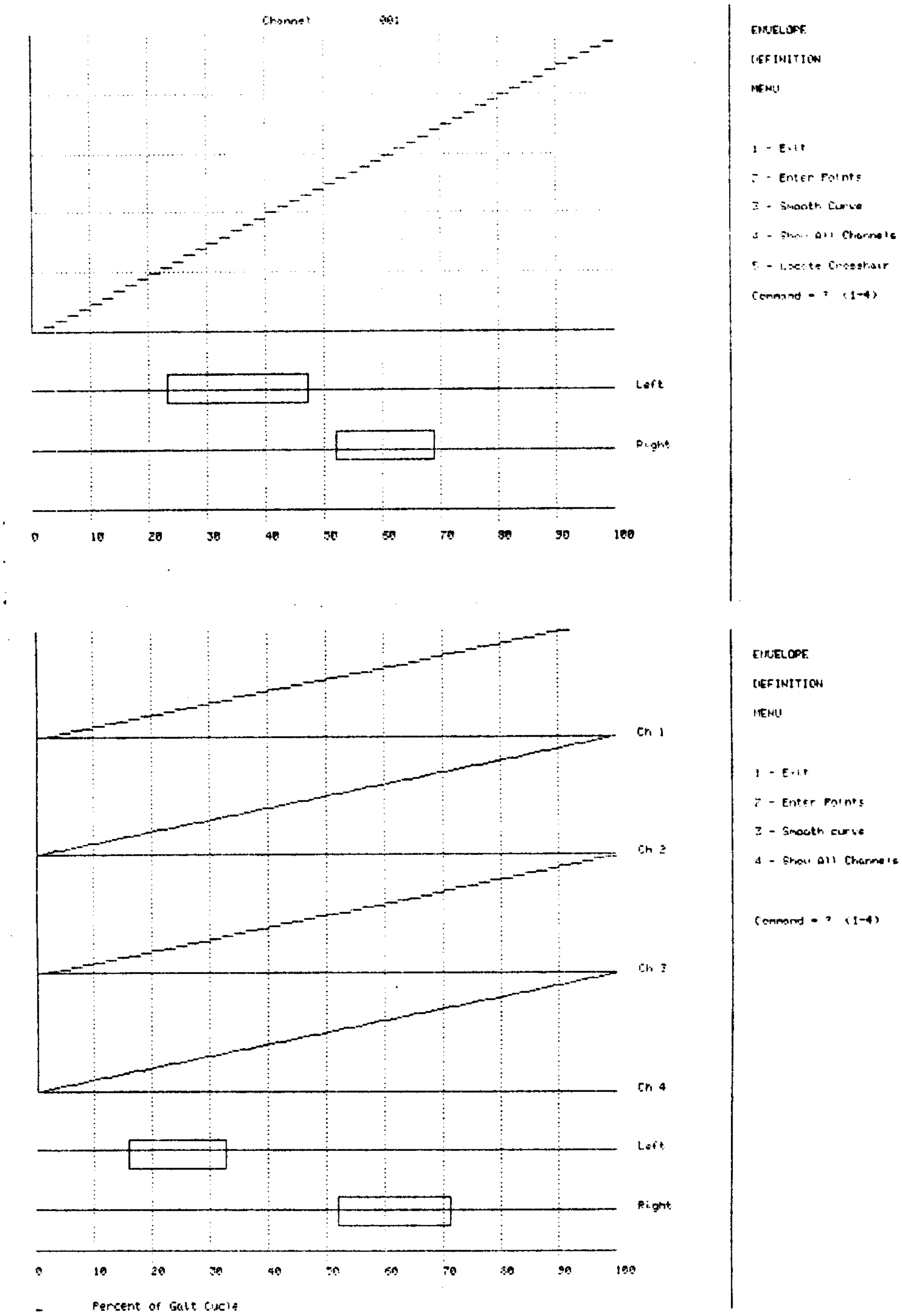

Figure 2. Sample of graphic display for envelope definition for a single channel and four channel summary information.

processor and only one or two dummy instructions need to be executed to wait long enough for the ADC data to be valid.

CONCLUSION

The above described system should prove to be an exceptionally powerful and flexible tool in our research for several years. The power of computer graphics and high level software languages such as Fortran will enable an ease of parameter definition heretofore unseen in a laboratory stimulation system. The speed of the slave processor and output module design coupled with assembly language control algorthms will allow numerous channels of output control while the host is free to acquire data and modify information used by the slave processor such that real time closed-loop control could eventually become a reality.

This system provides a fast, efficient way to alter many channels of stimulation during repeated walking trials with patients having neuromuscular impairments. The availability of such a system is imperative in selecting control sequences that will make a significant difference in the quality of walking for these individuals.

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